

# Subnanosecond Time-to-Digital Converter Implemented in a Kintex-7 FPGA

Yuta Sano, Yasuyuki Horii, Masahiro Ikeno, Osamu Sasaki, Makoto Tomoto, and Tomohisa Uchida

**Abstract**—Time-to-digital converters (TDCs) are used in various fields, including high-energy physics. One advantage of implementing TDCs in field-programmable gate arrays (FPGAs) is logics can be flexibly modified, which is useful to cope with unexpected problems and changes in the experimental conditions. Recent moderate FPGAs make it possible to implement TDCs with a subnanosecond bin size. Herein an eight-channel TDC with a variable bin size down to 0.28 ns is implemented and tested in a Xilinx Kintex-7 FPGA. The TDC is based on a multisampling scheme with quad phase clocks synchronised with an external reference clock. Calibration of the bin size is unnecessary if a stable reference clock is available, which is common in high-energy physics experiments. Depending on the channel, the standard deviation of the differential nonlinearity for a 0.28-ns bin size is 0.06–0.14 and the time resolution is 0.08–0.10 ns. The performance has a negligible dependence on the temperature. Power consumption and the potential to extend the number of channels are also discussed.

**Index Terms**—Field programmable gate arrays, Time-to-digital converter.

## I. INTRODUCTION

TIME-TO-DIGITAL converters (TDCs) are used in various fields, including high-energy physics. For example, in the ATLAS experiment [1], the muon momentum is measured with monitored drift tube chambers based on TDCs with a bin size of 0.78 ns, which are implemented in application-specific integrated circuits [2]. Moderate field-programmable gate arrays (FPGAs) make implementing TDCs with a nanosecond or small bin size possible [3], [4]. In many cases, the bin size of TDCs based on the propagation delay time must be calibrated to cope with the delay time dependence on the temperature as well as the location and routes of the delay units. On the other hand, the TDCs in this study, which are based on multi-phase clocks managed by a highly reliable clock manager integrated in the FPGA, do not require bin size calibration. Implementation of TDCs in FPGAs provides flexibility because logics can be modified to deal with unexpected problems and changes in the experimental conditions. Data transfer at a rate of gigabits per second can be handled with the robust transceivers integrated in FPGAs.

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In this study, an eight-channel TDC with a variable bin size down to 0.28 ns is implemented and tested in a Xilinx Kintex-7 FPGA [5]. The FPGA is XC7K325T-2FFG900 and has a speed grade of -2. This study extends the demonstration described in [6] by further analysing and interpreting the data as well as measuring the power consumption. Additionally, the potential to extend the number of channels to 256 is discussed.

## II. DESIGN OF THE TDC

Fig. 1 shows a block diagram of the TDC, which was designed to measure the timing of both the leading and the trailing edges of the input signal. The fine time measurement is based on free-running counters ('fine time counters'), which are designed with a multisampling scheme and quad phase clocks [7], [8], [9]. Each quad phase clock has a frequency one quarter of the fine time counters. The quad phase clocks are produced from an external reference clock at the clock manager integrated in the Kintex-7 FPGA, where the supported maximum frequency is 933 MHz. An external reference clock with a 110 MHz frequency corresponds to that of the quad phase clocks of 880 MHz and a 0.28-ns bin size.

The difference in the lengths of the divided input signal paths (see Fig. 1) is crucial for the TDC performance. In this study, the locations of the first four D-type flip-flops in each channel were constrained so that they are close to each other.

The data from the fine time counter includes a three-bit time count and a one-bit identifier of the leading and the trailing edges. These data are combined with the data from a fourteen-bit coarse time counter, and stored in a channel buffer. The channel buffers for all channels are scanned, and the data is transferred to a buffer with a five-bit channel identifier. Then the data are read out one by one. The dynamic range for a bin size of 0.28 ns is 37  $\mu$ s. The dynamic range can be extended by changing the number of bits for the coarse time counter.

## III. DEMONSTRATOR AND TEST SETUP

Fig. 2 shows a picture of the demonstrator, which consists of a motherboard and a daughter card. The motherboard is compatible with the versatile backplane bus standard VME [10]. It has a Kintex-7 FPGA (type is XC7K325T-2FFG900). Although either an onboard 40-MHz quartz oscillator or a LEMO coaxial connector [11] can provide the system clock, this study employed the latter. Additionally, the output from the FPGA can be read through the backplane or a gigabit Ethernet with a Transmission Control Protocol processor implemented in the FPGA (SiTCP) [12], but the latter was used. The daughter card has eight LEMO coaxial connectors as signal inputs. The input

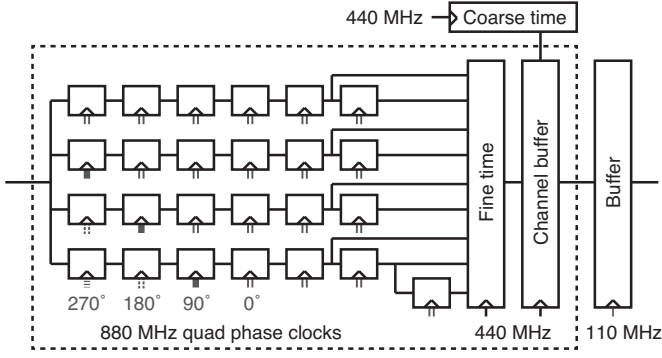


Fig. 1. Block diagram of the TDC. The signal path is divided into four, and the signal time is detected by the D-type flip-flops based on the four different clock phases. The locations of the four leftmost D-type flip-flops are constrained to control the difference between the divided signal paths. Each channel has a circuit, which is inside the square with the dashed line.

compatible with the NIM fast negative signal [13] is converted into a 3.3 V LVCMOS signal [14] with Texas Instruments SN65LVDS348PW [15]. Then the signal is transferred to the FPGA on the motherboard.

The signal and external reference clocks are from the pulse generator Agilent 81150A [16]. The standard deviation of the time difference between the leading edges of the two synchronised pulses from the pulse generator is 30 ps. The performances of bin sizes of 0.78 ns, 0.39 ns, and 0.28 ns, which correspond to the external reference clock frequencies of 40 MHz, 80 MHz, and 110 MHz, respectively, were evaluated. Unless otherwise specified, the results for the 0.28-ns bin size are shown. Although the leading edges were evaluated, the trailing edges should produce similar results since common clocks and D-type flip-flops are used.

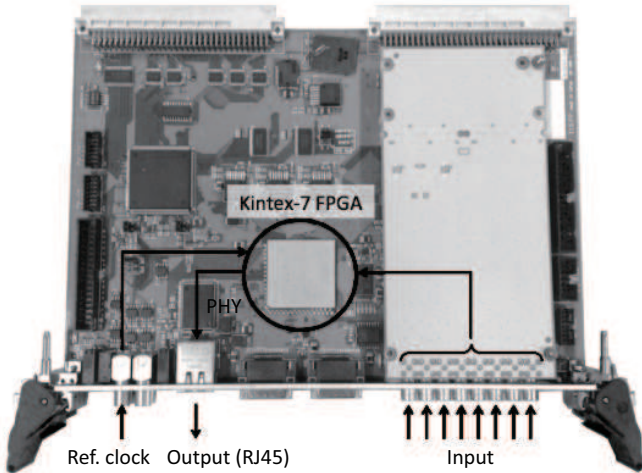


Fig. 2. Picture of the demonstrator.

#### IV. DIFFERENTIAL NONLINEARITY

The differential nonlinearity  $D_i$  is defined by

$$D_i = \frac{t_i - t_{\text{bin}}}{t_{\text{bin}}}, \quad (1)$$

where  $i$  ( $i = 0, 1, 2, \dots$ ) is the bin index,  $t_i$  is the bin size for bin  $i$ , and  $t_{\text{bin}}$  is the designed bin size. To evaluate  $D_i$ , the time difference of the leading edges between the signal and external reference clocks was measured. Multiple bins were investigated by scanning the time difference between the signal and external reference clocks with a 33-ps step size (Fig. 3). A periodic structure with a cycle of four bins was found. The maximum magnitude of the measured  $D_i$  is 0.6.

The delay  $\Delta_j$  before the first D-type flip-flop for each divided input signal path  $j$  ( $j = 0, 1, 2, 3$ ) was estimated by a Xilinx Vivado design tool. Based on the estimated delay, the bin size  $t_j$  for each quad clock phase  $j$  was calculated as

$$t_j = t_{\text{bin}} + \Delta_j - \Delta_{j+1}. \quad (2)$$

A cyclic relation of  $\Delta_4 = \Delta_0$  was used to calculate  $t_3$ . Table I shows the measured and calculated bin sizes for a channel. Fig. 4 shows the distribution of the difference between the measured and calculated bin sizes for all 32 quad clock phases of the 8 channels. The difference is O(0.01) ns, implying that the main source of the periodic structure in Fig. 3 is the difference in the divided input signal paths.

As a channel-level measure of  $D_i$ , the deviation  $\sigma$  is defined for each channel by

$$\sigma^2 = \frac{1}{N} \sum_{i=0}^{N-1} D_i^2, \quad (3)$$

where  $N$  is the total number of bins. Fig. 5 shows the result of the measurement of  $\sigma$ . The obtained value, which varies between 0.06–0.14, depends on the channel.

TABLE I  
RELATION BETWEEN THE CALCULATED AND THE MEASURED BIN SIZES.

Phase $j$	Input signal delay $\Delta_j$ [ns]	Calculated bin size [ns]	Measured bin size [ns]
0	4.62	0.20	0.21
1	4.70	0.20	0.20
2	4.79	0.34	0.36
3	4.73	0.39	0.37

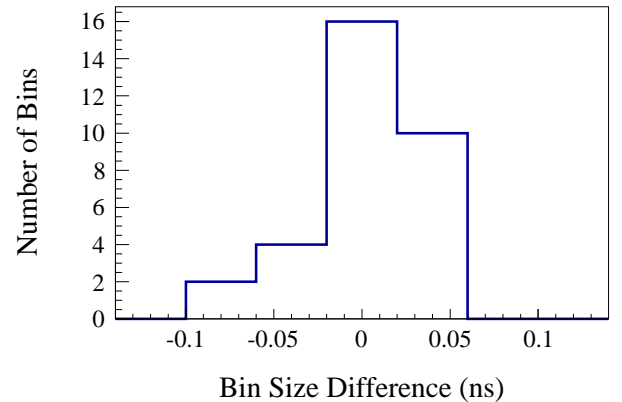
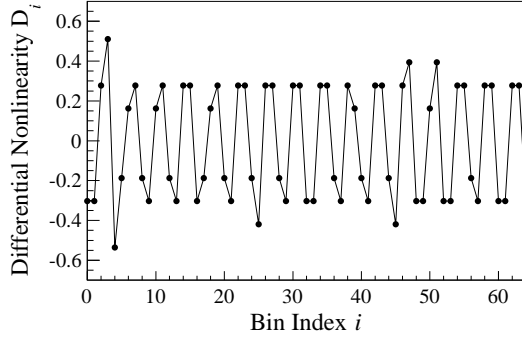
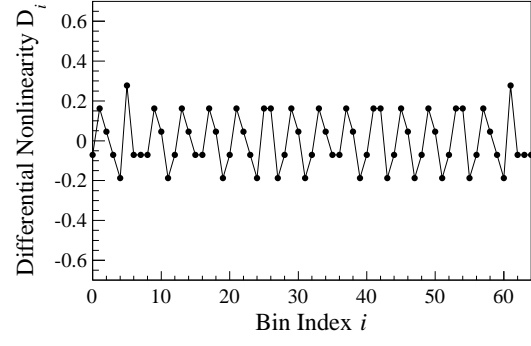
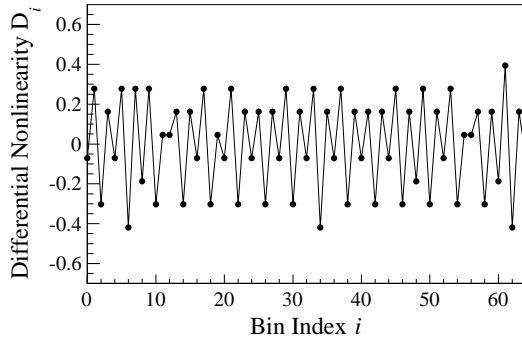
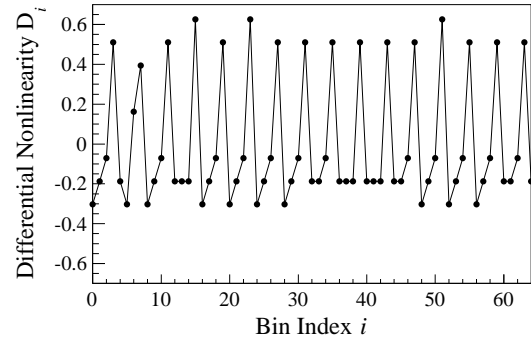
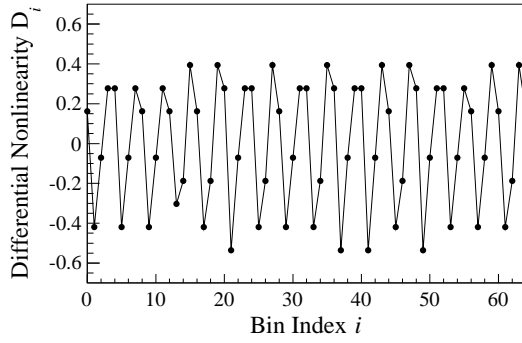
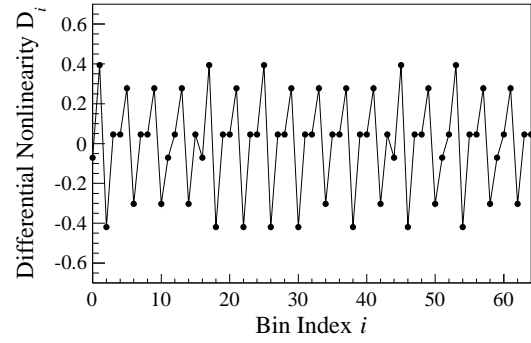
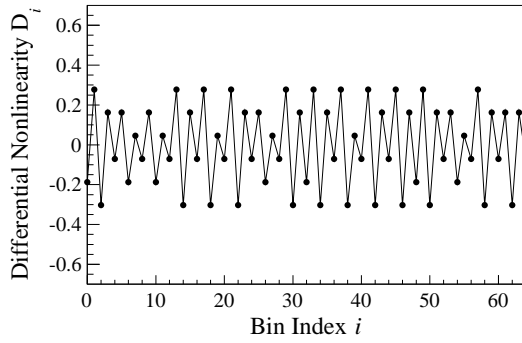
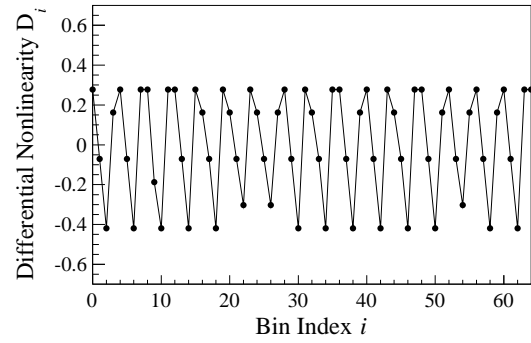
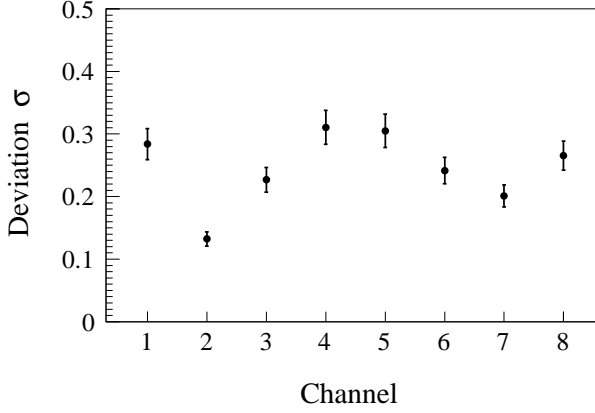


Fig. 4. Difference between the measured and calculated bin sizes.

(a) Differential nonlinearity  $D_i$  for channel 1.(b) Differential nonlinearity  $D_i$  for channel 2.(c) Differential nonlinearity  $D_i$  for channel 3.(d) Differential nonlinearity  $D_i$  for channel 4.(e) Differential nonlinearity  $D_i$  for channel 5.(f) Differential nonlinearity  $D_i$  for channel 6.(g) Differential nonlinearity  $D_i$  for channel 7.(h) Differential nonlinearity  $D_i$  for channel 8.Fig. 3. Result of the measurement of the differential nonlinearity  $D_i$ .

Fig. 5. Deviation  $\sigma$  of the differential nonlinearity.

### V. INTEGRAL NONLINEARITY

The integral nonlinearity  $I$  is given by

$$I = \frac{\langle T_{\text{measured}} \rangle - T_{\text{input}}}{t_{\text{bin}}}, \quad (4)$$

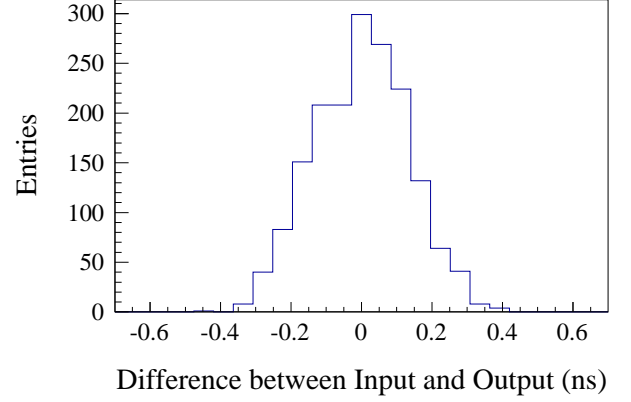
where  $T_{\text{input}}$  is the time difference between the leading edges of the input signal clock and  $\langle T_{\text{measured}} \rangle$  is the mean of the measurements. The time difference was scanned up to  $37 \mu\text{s}$ , and  $\langle T_{\text{measured}} \rangle$  is obtained for each time difference from 8500 measurements. The value of  $I$  is consistent with zero in the full range of the measurement, and the graph is fitted by a linear function  $I = A \cdot T_{\text{input}} + B$ . The fit results are shown in Fig. 6. The uncertainty of the slope parameter  $A$  corresponds to 1 ps over  $37 \mu\text{s}$ .

### VI. TIME RESOLUTION

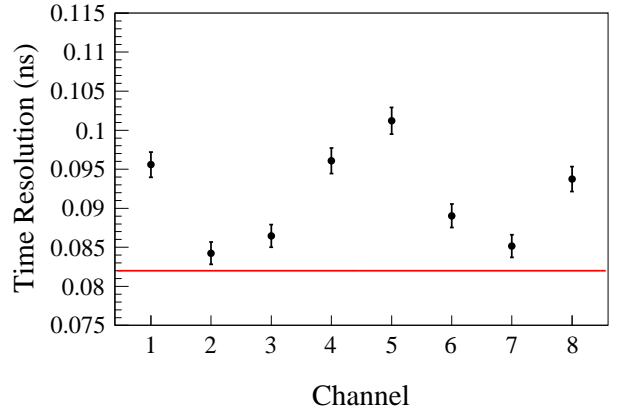
The time resolution was evaluated using data with various values of the time difference between the leading edges of the input signal clock. Specifically, the standard deviation of the difference between the measured and input time differences was examined (Fig. 7). The obtained value depends on the channel and ranges 0.08–0.10 ns. The result is fully correlated with the deviation  $\sigma$ , as seen by comparing Fig. 7 (b) and Fig. 5. The time resolution depends on the difference between the input signal paths. For larger bin sizes, the effect of the difference between the input signal paths relative to the quantisation error becomes smaller.

### VII. TEMPERATURE DEPENDENCE

The temperature dependences of  $D_i$  and  $I$  were evaluated with a thermostat chamber ESPEC SH-641 [17] for a temperature range from  $-10^\circ\text{C}$  to  $60^\circ\text{C}$ . The data were acquired after the temperature of FPGA became stable during the operation. The temperature of FPGA during operation is about  $8^\circ\text{C}$  higher than that of the chamber. Fig. 8 (a) shows the relation between the deviation  $\sigma$  of  $D_i$  and the temperature. Fig. 8 (b) shows the relation between the slope parameter  $A$  from the linear fit to  $I$  and the temperature. The temperature dependence is small in the investigated temperature range.



(a)



(b)

Fig. 7. (a) Distribution of the difference between the measured and input time difference. (b) Time resolution by channel. Line indicates the quantisation error.

### VIII. POWER CONSUMPTION

The power consumption of FPGA for the eight-channel TDC was estimated by the Vivado design tool. Table II summarises the results of  $28^\circ\text{C}$  and  $68^\circ\text{C}$  for bin sizes of 0.28 ns and 0.78 ns. The dominant contributors for the dynamic power consumption are found to be the clock manager and SiTCP, which spend about 40% and 30%, respectively. The power consumption for one-channel TDC was also estimated. Assuming a linear relation between the number of channels and the power consumption, the power consumption per channel for the bin sizes of 0.28 ns and 0.78 ns is 0.02 W and 0.01 W, respectively.

Fig. 9 shows the measured power consumption of the demonstrator. The measurement was performed with the thermostat chamber ESPEC SH-641 in a range from  $-10^\circ\text{C}$  to  $60^\circ\text{C}$ . The temperature of the FPGA during the measurement is about  $8^\circ\text{C}$  higher than that of the chamber. The measured power consumption for the 0.28-ns bin size at a chamber temperature  $20^\circ\text{C}$  is 4.1 W. The static power consumption of the demonstrator for the same bin size and temperature measured without firmware implemented in FPGA is 2.0 W. The dynamic power consumption of Texas

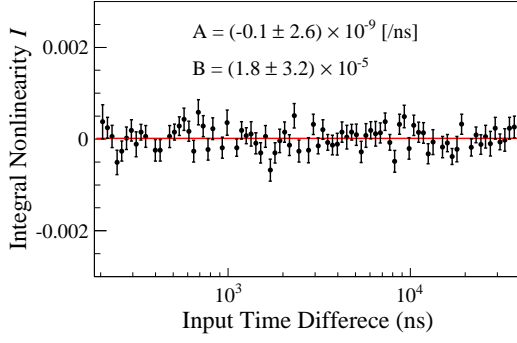
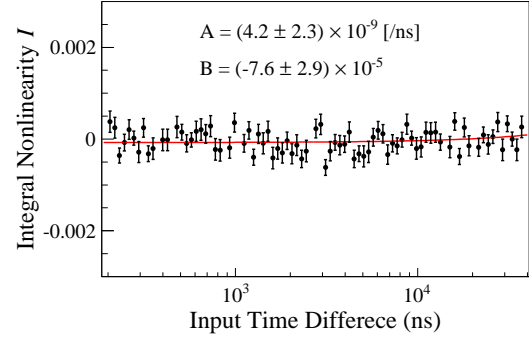
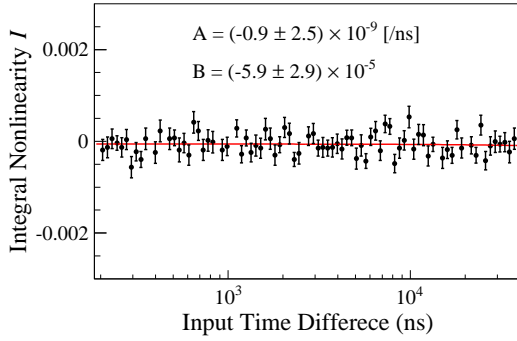
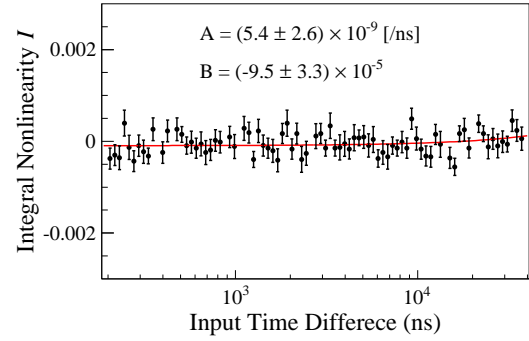
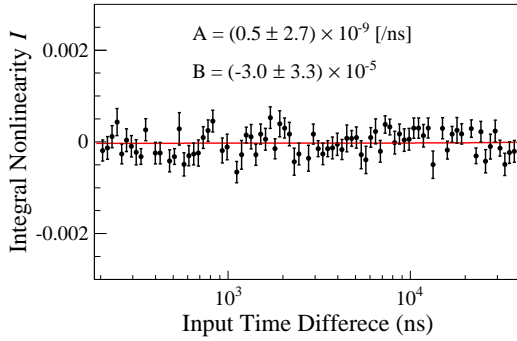
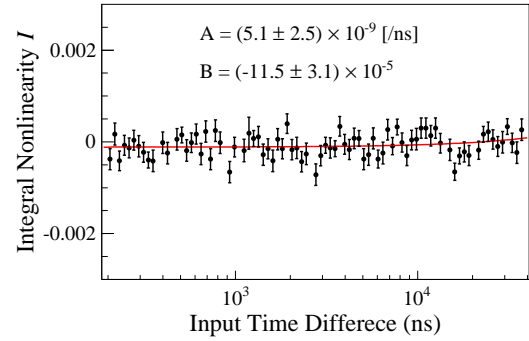
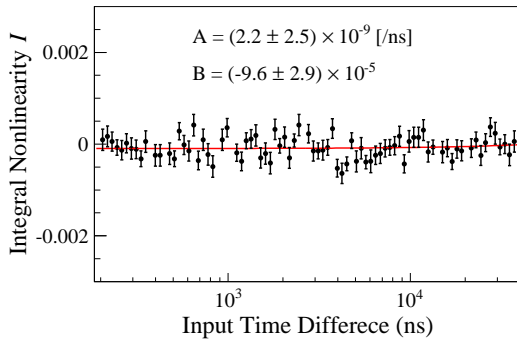
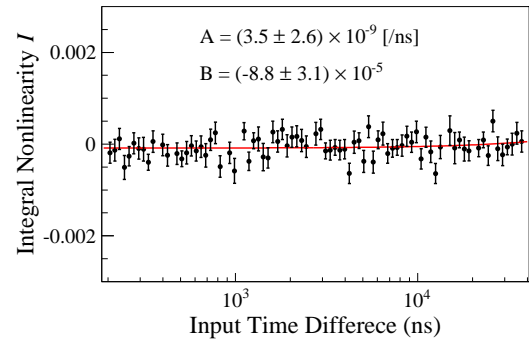
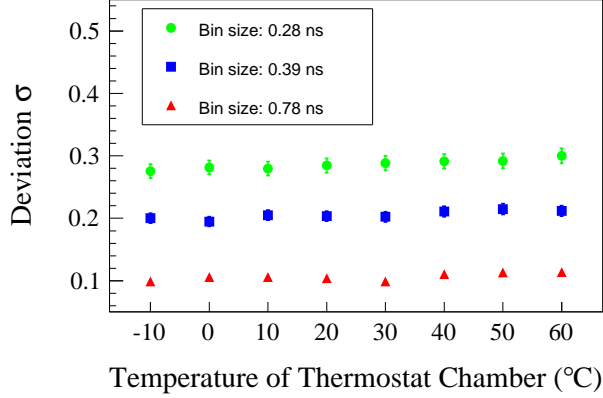
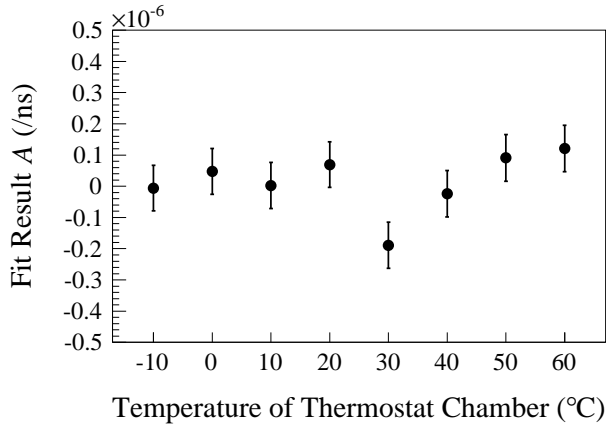
(a) Integral nonlinearity  $I$  for channel 1.(b) Integral nonlinearity  $I$  for channel 2.(c) Integral nonlinearity  $I$  for channel 3.(d) Integral nonlinearity  $I$  for channel 4.(e) Integral nonlinearity  $I$  for channel 5.(f) Integral nonlinearity  $I$  for channel 6.(g) Integral nonlinearity  $I$  for channel 7.(h) Integral nonlinearity  $I$  for channel 8.

Fig. 6. Result of the measurement of the integral nonlinearity  $I$ . Curves show the results of a linear fit by  $I = A \cdot T_{\text{input}} + B$ . Fitted values of parameters  $A$  and  $B$  are also shown for each plot.





(a)



(b)

Fig. 8. (a) Temperature dependence on the deviation  $\sigma$  of the differential nonlinearity for channel 8. Circle, square, and triangle plots correspond to bin sizes of 0.28 ns, 0.39 ns, and 0.78 ns, respectively. (b) Slope of the linear fit for the integral nonlinearity for channel 8 and a bin size of 0.28 ns.

Instruments DP83865DVH [15] for Ethernet data transfer, which is considered the main consumer on the demonstrator other than FPGA, is estimated to be 1.3 W. The value of  $4.1 \text{ W} - (2.0 \text{ W} + 1.3 \text{ W}) = 0.8 \text{ W}$  is close to the value estimated from the Vivado design tool of 0.73 W.

TABLE II  
POWER CONSUMPTION ESTIMATED BY THE XILINX DESIGN TOOL.

Bin size [ns]	Temp. [°C]	Dynamic [W]	Static [W]	Total [W]
0.28	28	0.56	0.18	0.73
0.28	68	0.56	0.59	1.15
0.78	28	0.43	0.18	0.61
0.78	68	0.43	0.59	1.02

## IX. RESOURCES AND NUMBER OF CHANNELS

Table III summarises the utilisation of the FPGA resources for the tested eight-channel TDC. Because multiple clocks with different frequencies are generated, the ratio of the utilised clock resources to the total clock resources is relatively large. Most of the resources of the look-up tables, the registers, and the random-access memory are spent by SiTCP.

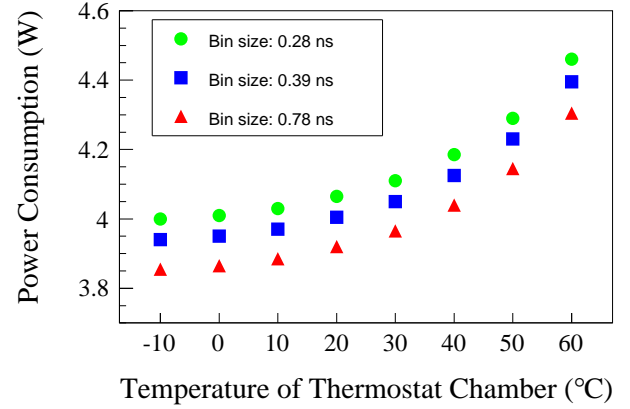


Fig. 9. Measured power consumption of the demonstrator during operation. Circle, square, and triangle plots correspond to bin sizes of 0.28 ns, 0.39 ns, and 0.78 ns, respectively.

To discuss the extension of the number of channels, we developed firmware with 256 channels and checked the utilised resources (Table IV). The ratio of the utilised input/output ports to the total input/output ports is 58%, while the ratios for the other elements are smaller. The difference in the divided input signal delay for each channel was evaluated by the Vivado design tool. The standard deviation of the input signal delay is 0.14 ns, indicating that the performance of the 256-channel TDC should be similar to the one of the eight-channel TDC demonstrated in this study. The clock skew may affect the offset between the channels, but it is within a range supported for the employed Kintex-7 FPGA.

TABLE III  
UTILISATION OF THE FPGA RESOURCES FOR EIGHT-CHANNEL TDC.

Resource	Utilisation	Available	Ratio [%]
Look-up tables	4361	203800	2.1
Registers	5939	407600	1.5
Memory	48	445	10.8
Input/output ports	60	582	10.3
Clocking	14	32	43.8

TABLE IV  
UTILISATION OF THE FPGA RESOURCES FOR 256-CHANNEL TDC.

Resource	Utilisation	Available	Ratio [%]
Look-up tables	27682	203800	13.6
Registers	48826	407600	12.0
Memory	180	445	40.4
Input/output ports	292	582	58.4
Clocking	14	32	43.8

## X. CONCLUSION

An eight-channel TDC with a variable bin size down to 0.28 ns was implemented and tested in a Xilinx Kintex-7 FPGA. The TDC is based on a multisampling scheme with quad phase clocks synchronised with an external reference clock. The measured time resolution for a 0.28-ns bin size is 0.08–0.10 ns, depending on the channel. The performance has

a negligible dependence on the temperature. The number of channels can be increased up to hundreds of channels without significantly changing the TDC performance.

Implementation of TDCs in FPGAs increases the flexibility to modify logics. This feature is extremely advantageous when coping with unexpected problems or changes in the experimental conditions. If a stable reference clock is available such as in high-energy physics experiments, the TDC in this study does not need to be calibrated. Consequently, FPGA-based TDCs should be useful in fields requiring subnanosecond resolution and multiple channels.

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